

DESIGN OF DIGITAL ASYNCHRONOUS SEQUENTIAL SYSTEM USING PULSE MODE AND LEVEL SIGNALS INPUTS

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Abstract: In this paper we propose to present the pulse mode asynchronous sequential systems implementation method. On the system input we have digital level input signals and pulses signals inputs. During the pulses inputs are generated, the digital level input signal must remain constant (1 or 0). If it changes it's value during the pulses occurrences, the system may fail. To generate de pulses signals we use relays switchers. The proposed algorithm can be successfully implemented in vending machines automata.

Keywords: Asynchronous Sequential System, Level Signal, Pulses Signals, Master-Slave, Latches, R-S, digital logic, ModelSim, VHDL.

1. INTRODUCTION

A typical case for an asynchronous digital system is where the inputs are for two types: statics and pulses. The pulse input signal is equivalent with the synchronous sequential system's clock signal. For example, a cigars, chocolate, drink vending machine where the coins produce the input pulse who controll the selection and releasing of the product.

The digital systems with one or many input pulses signals we will name digital asynchronous sequential systems with pulses inputs or multiple clocks digital asynchronous sequential systems.

Lets consider the equaions of digital system like:

$$\begin{aligned}
 x &= \{x_{r-1}, \dots, x_0\} - \text{level input signals} \\
 p &= \{p_{q-1}, \dots, p_0\} - \text{pulse input signals} \\
 y &= \{y_{n-1}, \dots, y_0\} - \text{state signals} \\
 z &= \{z_{m-1}, \dots, z_0\} - \text{output signals}
 \end{aligned}
 \tag{1}$$

A such system implemented with CBB-D type is illustrating next, figure 1.

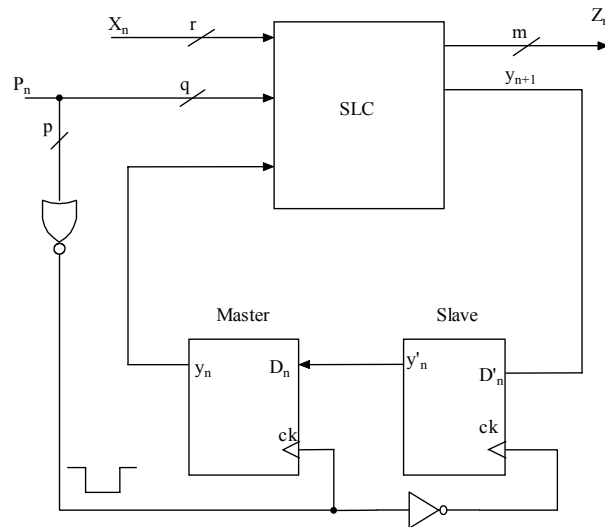


Figure 1. Pulse Mode Automata Design

The circuits notated with M, S are latch CBB-D, it's necessary that one time just one input pulse signal (P_i) to be activated, (2).

$$\sum_{k=0}^{q-1} P_k = 0 \text{ or } \sum_{k=0}^{q-1} P_k = 1 \text{ cu } P_i \cdot P_k = 0, k \neq i, P_i = 1 \quad (2)$$

Lets implement an asynchronous sequential system who has pulse mode inputs, logic level inputs and logic outputs.

Figure 2 shows these inputs:

- x- logic level input (1 or 0);
- A,B,R – pulses inputs
- z1,z0 - logic outputs

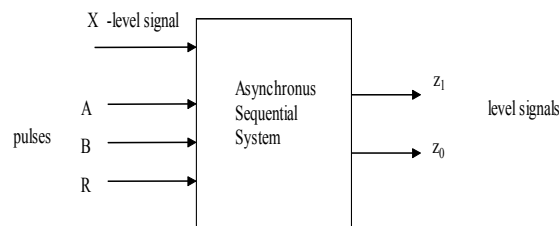


Figure 2. Automata Design

2.ASYNCHRONOUS SEQUENTIAL SYSTEM DESIGN

We propose to implement a semaphore system which contains two leds (read and green). These two leds are connected to the outputs signals on to the following ways:

- $Z1=1$ means that the green led will be ON
- $Z1=0$ means that the green led will be OFF

- $Z_0=1$ means that the red led will be ON
- $Z_0=0$ means that the red led will be OFF.

The green led will be ON only when the x level input signal is 1, ($x=1$), and the pulses sequence ABAR will be executed, figure 3.

The red led will be ON only when the x level input signal is 0, ($x=0$), and the pulses sequence ABAR will be executed, figure 3.

	z_1 Led Verde	z_0 Led Rosu
$x=1$	ON	OFF
$x=0$	OFF	ON

Figure 3. Automata Signals

The value of level input must be constant all the period of time on pulses occurrences. This condition is essential for good working of the digital system.

We use an astabil circuit for the generating of the x input signals, figure 4. It let us to stabilize the minim and maxim timing input x signal, these timing values need to be respected.

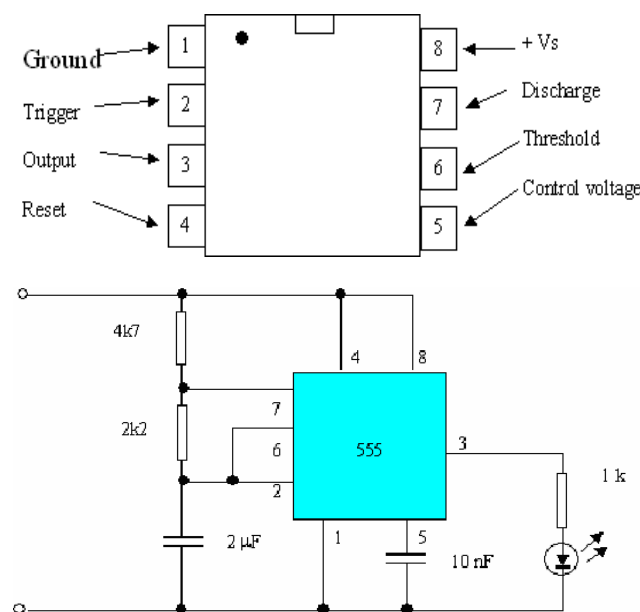


Figure 4. Using The Astabil Implementation

The pulses generated by the astabil circuit for the X level input logic are showing in figure 5.

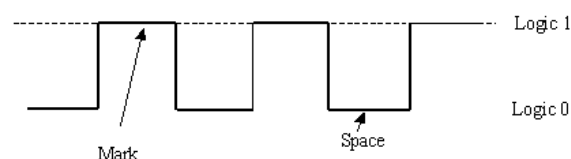


Figure 5. Generating x Level Signals

The generated frequency for the x signal is calculated like on (3):

$$f = \frac{1.4}{(R_1 + 2 \cdot R_2) \cdot C} \quad (3)$$

Using the values like $R_1 = 4700\Omega$, $R_2 = 2200\Omega$, $C = 2.0 \times 10^{-6} F$ we obtain the (4) equation.

$$f = \frac{1.4}{[4700 + (2 \cdot 2200)] \times 2.0 \times 10^{-6}} = \frac{1.4}{9100 \times 2.0 \times 10^{-6}} = 77Hz \quad (4)$$

The R,A,B signals are generated by relay switching circuits. The entire system has 9 states, the synthesis and implementation of these states are not so reasonable, so we divide the automata in 2 small automata, A1 and A0. A1 will do the algorithm for the Z1=1 means green led ON and A0 will do the algorithm for the Z0=1 means red led ON, figure 6.

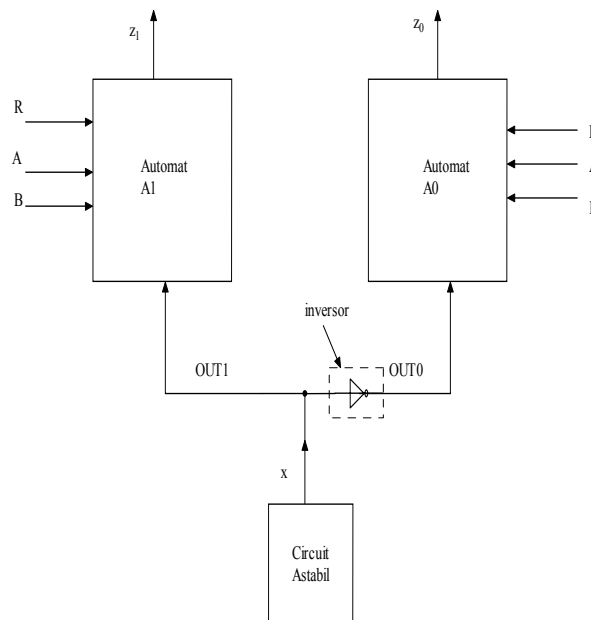


Figure 6. Automata Design

The A1 automata fluence graph is described in figure 7.

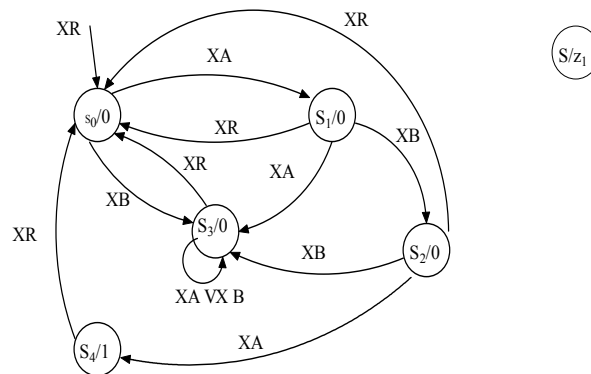


Figure 7. A1 Automata States Graph

The equations for the R-S latch implementation are, (5).

$$\begin{aligned}
 S_2 &= X \cdot A \cdot y_1 \cdot y_0 \\
 R_2 &= X \cdot R \\
 S_1 &= X \cdot (A \cdot y_0 + B) \\
 R_1 &= X \cdot R \\
 S_0 &= X \cdot A \cdot \overline{y_1} \cdot \overline{y_0} \\
 R_0 &= X \cdot (A \cdot y_0 + B \cdot y_1 + R) \\
 Z_1 &= X \cdot (y_2 y_1 \overline{y_0})
 \end{aligned} \tag{5}$$

From the (5) equation results that the x logic level signal need to be 1 logic all these time. On the end of the algorithm, the green led will be ON.

The fluence graph table for the A0 automata is described in figure 8.

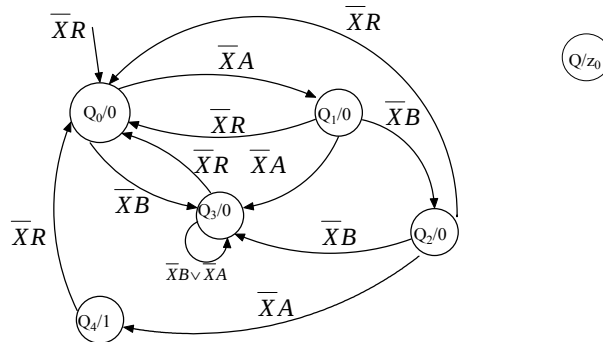


Figure 8.A0 Automata States Graph

The equation for the R-S latch implementation are, (6).

$$\begin{aligned}
 S_2^* &= \overline{X} \cdot A \cdot y_1 \cdot y_0 \\
 R_2^* &= \overline{X} \cdot R \\
 S_1^* &= \overline{X} \cdot (A \cdot y_0 + B) \\
 R_1^* &= \overline{X} \cdot R \\
 S_0^* &= \overline{X} \cdot A \cdot \overline{y_1} \cdot \overline{y_0} \\
 R_0^* &= \overline{X} \cdot (A \cdot y_0 + B \cdot y_1 + R) \\
 Z_0 &= \overline{X} \cdot (y_2 y_1 \overline{y_0})
 \end{aligned} \tag{6}$$

The figure 9 shows the timing analysis generated by ModelSim 5.8e using the VHDL Hardware Description Language.

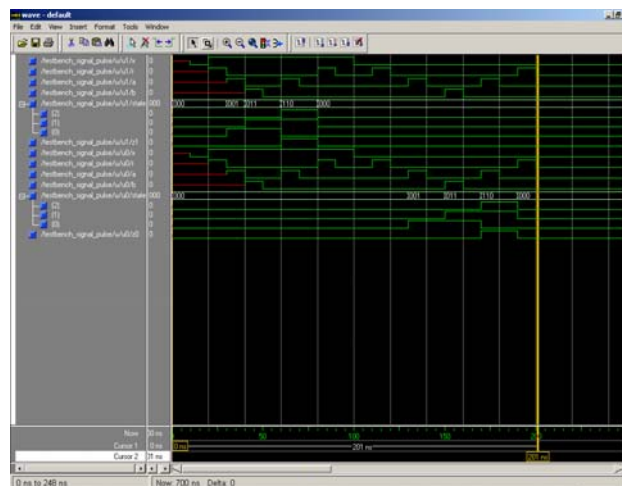


Figure 9. Timing Diagram Charts

3.CONCLUSIONS

The proposed system for synthesis and implement using the pulse mode specifications can be used in a large area of digital systems especially on asynchronous digital systems. Such a asynchronous digital systems are by example vending machines, semaphores.

As we demonstrated, the proposed algorithm was successfully implemented in an asynchronous digital semaphore system.

4.REFERENCES

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