DESIGN OF DIGITAL ASYNCHRONOUS SEQUENTIAL SYSTEM USING ONLY PULSE MODE INPUTS

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Abstract: In this paper we propose to present the pulse mode asynchronous sequential systems implementation method. On the system input we have digital level input signals and pulses signals inputs. During the pulses inputs are generated, the digital level input signal must remain constant (1 or 0). If it changes it's value during the pulses occurrences, the system may fail. To generate de pulses signals we use relays switchers. The proposed algorithm can be successfully implemented in vending machines automata.

Keywords: Asynchronous Sequential System, Level Signal, Pulses Signals, Master-Slave, Latches, R-S, digital logic, ModelSim, VHDL.

1.INTRODUCTION

A tipical case for an asynchronous digital system is where the inputs are for two types: statics and pulses. The pulse input signal is equivalent with the synchronous sequential system's clock signal. For exeample, a cigars, chocolate, drink vending machine where the coins produce the input pulse who controll the selection and releasing of the product.

The digital systems with one or many input pulses signals we will name digital asynchronous sequential systems with pulses inputs or multiple clocks digital asynchronous sequential systems.

Let consider the equaions of digital system like:

$$\begin{aligned} x &= \{x_{r-1},...x_0\} \text{ - level input signals} \\ p &= \{p_{q-1},...p_0\} \text{ - pulse input signals} \\ y &= \{y_{n-1},...y_0\} \text{ - state signals} \\ z &= \{z_{m-1},...z_0\} \text{ - output signals} \end{aligned} \quad (1)$$

A such system implemented with CBB-D type is ilustrating next, figure 1.

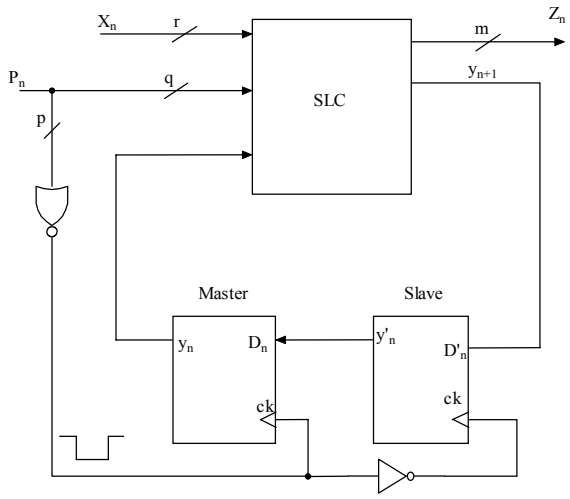


Figure 1.Pulse Mode Automata Design

The circuits notated with M, S are latch CBB-D, it's necessary that one time just one input pulse signal (P_j) to be activated, (2).

$$\sum_{k=0}^{q-1} P_k = 0 \text{ or}$$
$$\sum_{k=0}^{q-1} P_k = 1 \text{ cu } P_i \cdot P_k = 0, k \neq i, P_i = 1 \tag{2}$$

2.ASYNCHRONOUS SEQUENTIAL SYSTEM DESIGN

Lets consider a digital system that will detects a vector of input signals like R A B A R. When the digital system detects this sequence of signals, it generates a Z=1 output signal All the input signals are asynchronous, they aren't synchronize with any clock driving signal, figure 2.

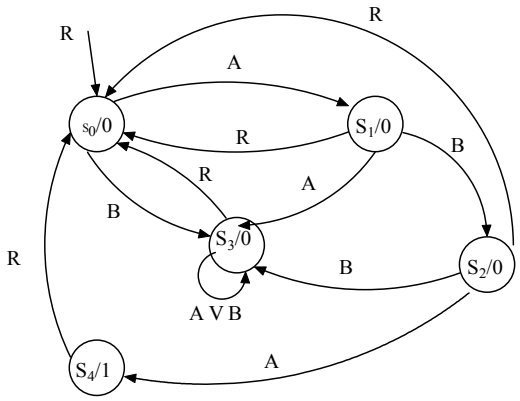


Figure 2.Automata States Graph

For the synthesis of the digital system, I will you the modified Veitch-Karnaugh methid. If we have k input pulse signals notaed with P_i and *n signals* S_i, so we will have k*2^n columns in Veitch-Kranaugh modiefied method, figure 3, figure 4.

$y_2y_1y_0$	A	B	R	Z
S0	S1	S3	S0	0
S1	S3	S2	S0	0
S2	S4	S3	S0	0
S3	S3	S3	S0	0
S4	-	-	S0	1
S5	-	-	-	-
S6	-	-	-	-
S7	-	-	-	-

Figure 3.Fluence Automata States Table

St.- y2y1y0	R	A	R	Z
S1 – 000	001	010	000	0
S2 – 001	010	011	000	0
S3 – 011	110	010	000	0
S4 – 010	010	010	000	0
S5 – 110	---	---	000	1
S6 – 111	---	---	---	-
S7 – 101	---	---	---	-
S8 –100	---	---	---	-

Figure 4.Automata Transitions Table

Using the R-S circuits equations, we will have, (3):

$$\begin{aligned} S_2 &= A \cdot y_1 \cdot y_0 \\ R_2 &= R \\ S_1 &= A \cdot y_0 + B \\ R_1 &= R \\ S_0 &= A \cdot \overline{y_1} \cdot \overline{y_0} \\ R_0 &= A \cdot y_0 + B \cdot y_1 + R \end{aligned} \tag{3}$$

The output signal equation will be:

$$Z = y_2 y_1 \overline{y_0} \tag{4}$$

The Figure 5 presents the digital system design analisys with Master-Slave circuits.

When a pulse input signal is generated, the output signal can't be read because the slave circuits are blocked. When the input pulse signals are off, the Slaves circuits are opened and the next state can be read, (Q_{n+1}). The output signals values can be read only when the input pulse signals are off. The proposed desing for the asynchronous digital system is working well on the proposed digital system. It can be successfully implemented on every digital asynchronous system.

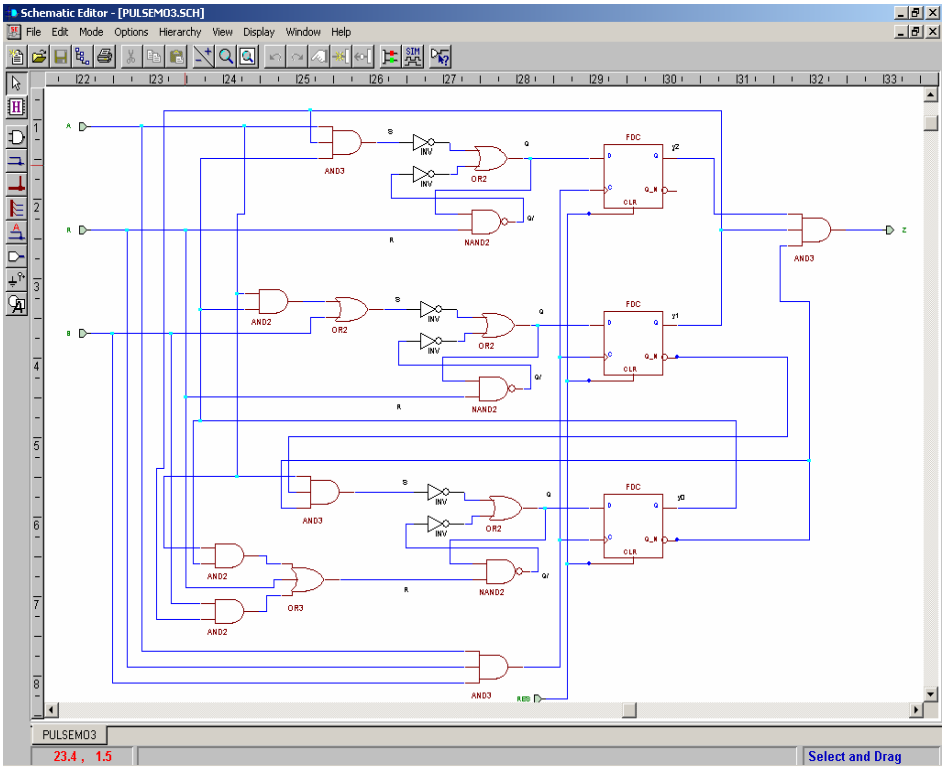
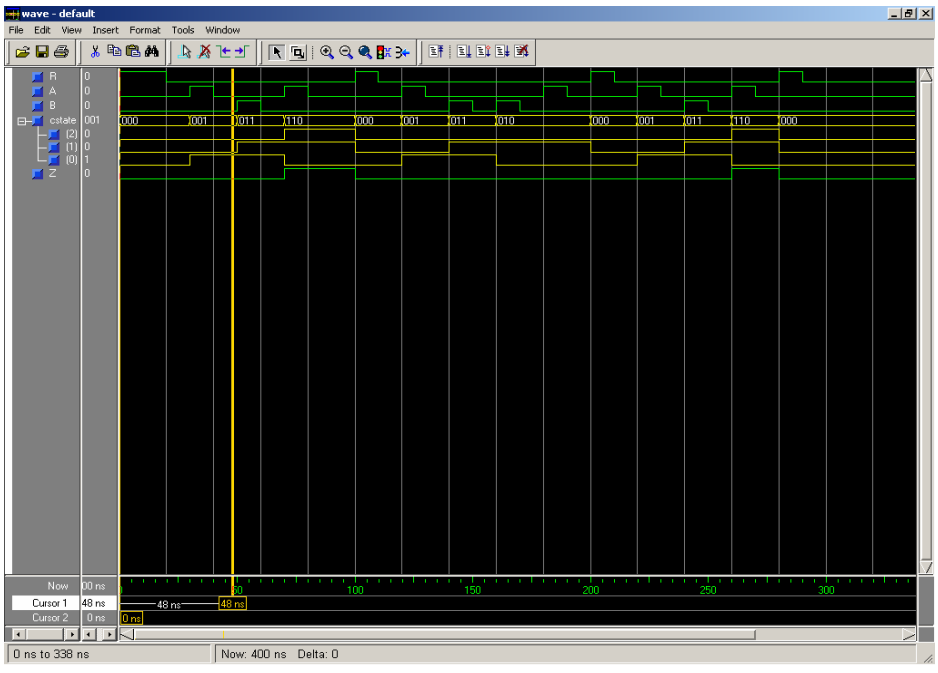


Figure 5.Schematic Design



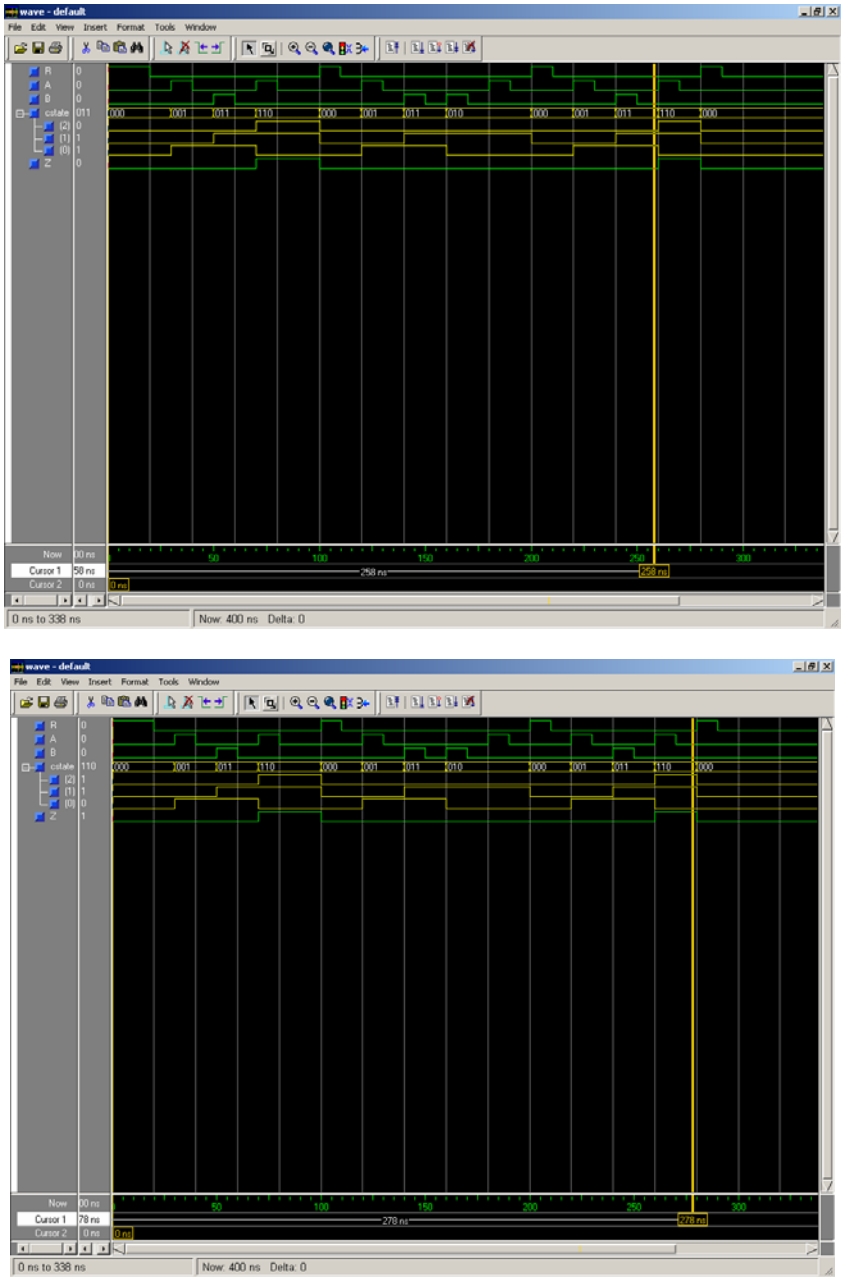


Figure 6.Timing Analysis

3.CONCLUSIONS

The proposed system for synthesis and implement using the pulse mode specifications can be used in a large area of digital systems especially on asynchronous digital systems. Such a asynchronous digital systems are by example vending machines, semaphores.

As we demonstrated, the proposed algorithm was successfully implemented in an asynchronous digital semaphore system.

4.REFERENCES

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